



SANYO Semiconductors

## DATA SHEET

# LA6569 — Monolithic Linear IC

## 5-channel Driver for Compact Disk Applications

### Overview

The LA6569 is a 5-channel driver for optical disc drives that includes a regulator on/off circuit.

### Features

- Power amplifier 5-channel built-in. (Bridge-connection (BTL) : 4-channel, H bridge : 1-channel)
- $I_O$  max 1A.
- Level shift circuit built-in (except H bridge).
- Mute circuit (output ON/OFF) built-in.  
(Operable with BTL AMP with MUTE1 : CH1 and MUTE2 : CH2 to 4 and not operable for the H bridge of 3.3VREG.)
- 3.3V regulator built-in (external PNP transistor).
- With a function to set the loading output voltage.
- Overheat protection circuit (thermal shutdown) built-in.
- Regulator ON/OFF circuit built-in.

### Specifications

#### Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC}$ max		14	V
Maximum output current	$I_O$ max	Each output for H bridge, channel 1 to 4	1	A
Maximum input voltage	$V_{INB}$ max		13	V
Mute pin voltage	$V_{MUTE}$		13	V
Allowable operation	$P_d$ max	Independent IC	0.8	W
		*Mounted on a standard board	2.0	W
Operating temperature	$T_{opr}$		-30 to +85	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +150	$^\circ\text{C}$

\*1 A circuit board for mounting (76.1mm×114.3mm×1.6mm, glass epoxy resin)

#### Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
supply voltage	$V_{CC}$	Same for $V_{CC}$ -VREG	4.5 to 13	V

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**SANYO Semiconductor Co., Ltd.**

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

## LA6569

**Electrical Characteristics** at  $T_a = 25^\circ\text{C}$ ,  $V_{CC1} = V_{CC2} = 8\text{V}$ ,  $V_{REF} = 1.65\text{V}$ , unless especially specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
All blocks						
No-load current drain ON	$I_{CC-ON}$	FWD = REV = 0, All outputs ON *1		30	50	mA
No-load current drain OFF	$I_{CC-OFF}$	FWD = REV = 0, All outputs OFF *1		10	20	mA
VREF input voltage range	$V_{REF-IN}$		1		$V_{CC}-1.5$	V
Thermal shutdown temperature	TSD	*2	150	175	200	$^\circ\text{C}$
BTL AMP block (CH1 to CH4)						
Output offset voltage	$V_{OFF}$	Voltage difference between outputs for BTL AMP, each channel. *3	-60		60	mV
Input voltage range	$V_{IN}$	Input voltage range for input for OP-AMP.	0		$V_{CC}-1.5$	V
Output voltage	$V_O$	Each voltage between $V_{O+}$ and $V_{O-}$ when $R_L = 8\Omega$ . *4	5.7	6.5		V
Closed-circuit voltage gain	VG	Input and output gain. *3	5.4	6	6.6	deg
Slew rate	SR	AMP Independent. Multiply 2 between outputs. *2		0.5		$\text{V}/\mu\text{s}$
MUTE ON voltage	$V_{MUTE-ON}$	Each MUTE *5	2			V
MUTE OFF voltage	$V_{MUTE-OFF}$	Each MUTE *5			0.5	V
Input AMP block (CH1 to CH4)						
Input voltage range	$V_{IN-OP}$		0		$V_{CC}-1.5$	V
Output current (SINK)	$SINK-OP$		2			mA
Output current (SOURCE)	$SOURCE-OP$	*6	300	500		$\mu\text{A}$
Output offset voltage	$V_{OFF-OP}$		-10		10	mV
Loading block (CH5, H bridge)						
Output voltage	$V_{O-LOAD}$	Forward, reverse, $R_L = 8\Omega$ *4	5.7	6.5		V
Break output saturation voltage	$V_{CE-BREAK}$	Output voltage at braking *7			0.3	V
Input low level	$V_{IN-L}$				1	V
Input high level	$V_{IN-H}$		2			V
Output set voltage	VCONT	$I_O = 200\text{mA}$ (Between outputs), $V_{CONT} = 3\text{V}$	2.9	3.15	3.4	V
Power supply block (PNP transistor : 2SB632K-use)						
3.3V supply output	$V_{OUT}$	$I_O = 200\text{mA}$	3.15	3.3	3.45	V
REG-IN SINK current	REG-IN-SINK	Base current to external PNP *8		10		mA
Line regulation	$\Delta\text{VOLN}$	$6\text{V} \leq V_{CC} \leq 12\text{V}$		20	150	mV
Load regulation	$\Delta\text{VOLD}$	$5\text{mA} \leq I_O \leq 200\text{mA}$		50	200	mV
Regulator ON	REG-EN-ON	Regulator ON *9	2			V
Regulator OFF	REG-EN-OFF	Regulator OFF *9			0.5	V

\*1. Current dissipation that is a sum of  $V_{CC1}$  and  $V_{CC2}$  at no load.

\*2. Design guarantee value.

\*3. Input AMP is a BUFFER AMP.

\*4. Voltage difference between both ends of load ( $8\Omega$ ). Output saturated.

\*5. Output ON with MUTE : [H] and OFF with MUTE : [L] (HI impedance).

\*6. The source of input OP-AMP is a constant current. As the  $11\text{k}\Omega$  resistance to the next stage is a load, pay due attention when setting the input OP-AMP gain.

\*7. Short (GND) brake used. SINK side output ON.

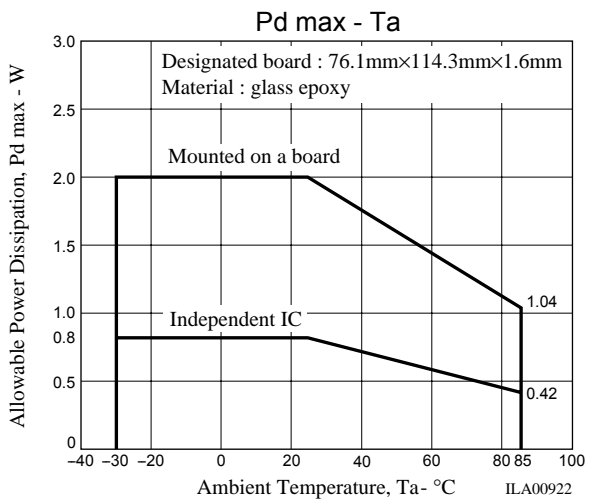
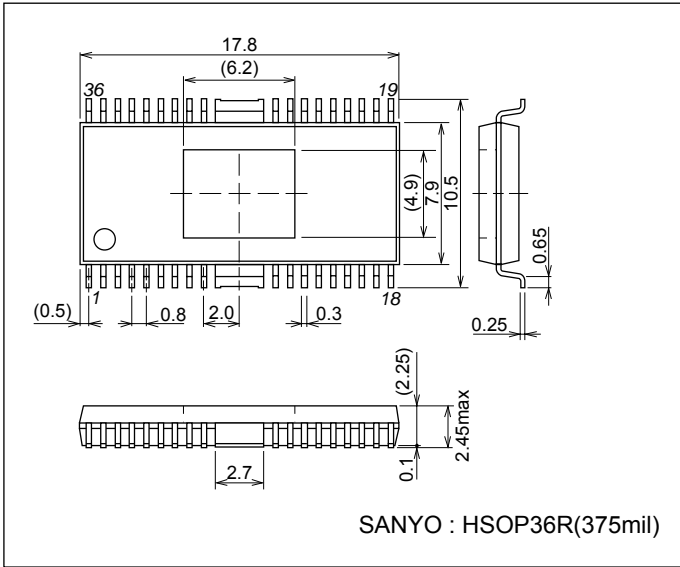
\*8. 3.3VREG incorporates a drooping protection circuit and operated when the base current is  $10\text{mA}$  (TYP).

\*9. The output is  $3.3\text{V}$  when the REG-EN pin is HIGH.

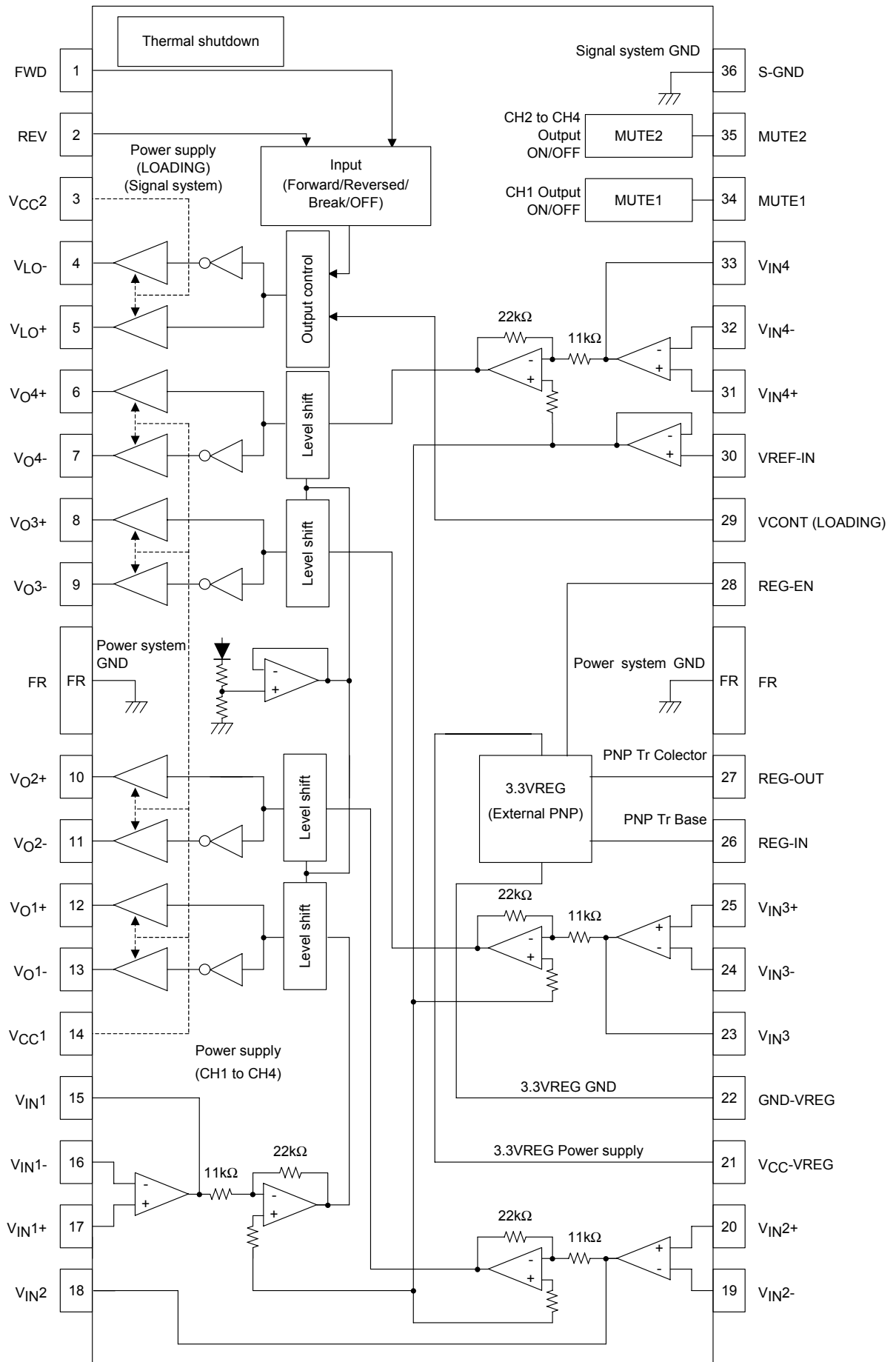
Package Dimensions

unit : mm

3251



Block Diagram

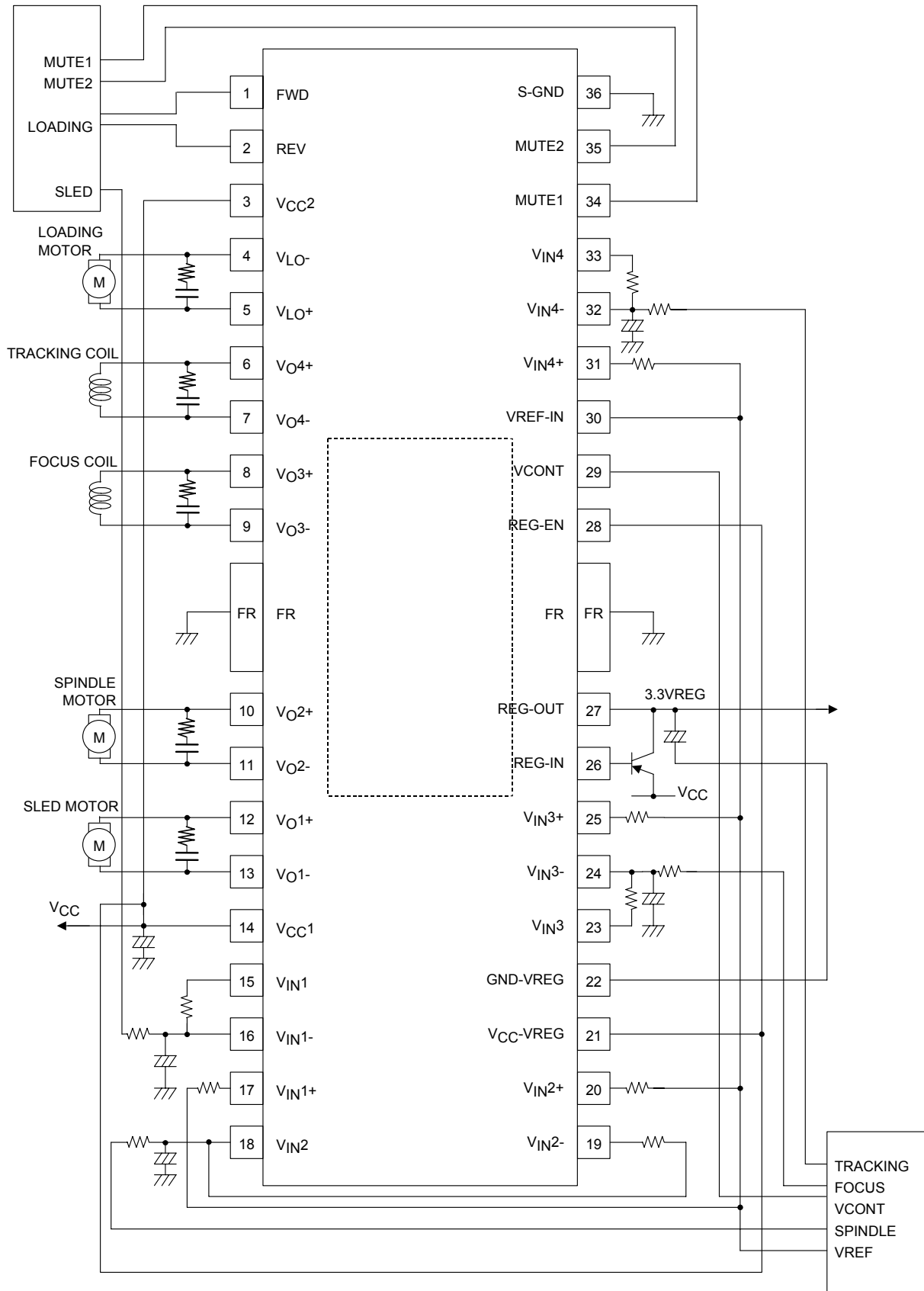


# LA6569

## Pin Description

Pin name	Pin name	Pin no.	Equivalent circuit	Pin explanation
Input (CH1 to 4)	V <sub>IN1+</sub> V <sub>IN1-</sub> V <sub>IN1</sub> V <sub>IN2+</sub> V <sub>IN2-</sub> V <sub>IN2</sub> V <sub>IN3+</sub> V <sub>IN3-</sub> V <sub>IN3</sub> V <sub>IN4+</sub> V <sub>IN4-</sub> V <sub>IN4</sub>	17 16 15 20 19 18 25 24 23 31 32 33		Input pin (CH1 to 4).
Input (LOADING)	FWD REV	1 2		Logic input pin. By combining H and L of this pin, any one of four modes (forward/reversed/brake/idling) can be selected.
Output (CH1 to 4)	V <sub>O1+</sub> V <sub>O1-</sub> V <sub>O2+</sub> V <sub>O2-</sub> V <sub>O3+</sub> V <sub>O3-</sub> V <sub>O4+</sub> V <sub>O4-</sub>	12 13 10 11 8 9 6 7		Output for channel 1 to 4.
MUTE	MUTE1 MUTE2	34 35		BTL AMP output. Output ON/OFF for CH1 to CH4. MUTE: H output ON MUTE: L output OFF
Output (LOADING)	V <sub>LO+</sub> V <sub>LO-</sub>	5 4		Output voltage set pin for loading block.

Sample Application Circuit



Note : Add CR between outputs or to a circuit to GND when oscillation occurs in the output.  
 Apply 4.5V or more to the external PNPT<sub>r</sub> emitter pin.

**Truth Table (loading (H bridge) section)**

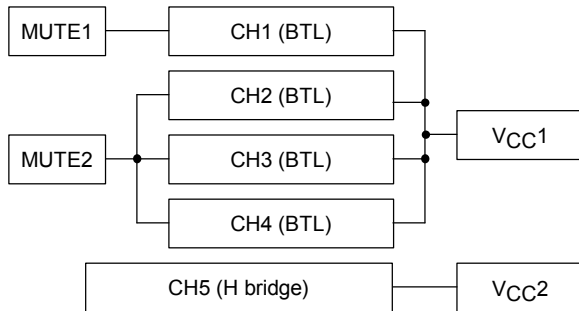
FWD	REV	Loading output
L	L	OFF *1
	H	Forward
H	L	Reversed
	H	(Short) brake *2

\*1 The output has a high impedance.

\*2 At brake, the SINK side transistor is ON (short brake).

$V_{LO+}$  and  $V_{LO-}$  are approximately on the GND level.

**Relation of MUTE and Power ( $V_{CC}^*$ )**



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